

## CLAIMS

1. A method for fabricating an ultra-shallow surface channel MOS transistor, the method comprising:  
forming CMOS source and drain regions, and an intervening  
5 well region with a surface;  
depositing a surface channel on the surface overlying the well region;  
forming a high-k dielectric overlying the surface channel;  
and,  
10 forming a gate electrode overlying the high-k dielectric.

2. The method of claim 1 wherein depositing a surface channel on the surface overlying the well region includes depositing a metal oxide surface channel material.

3. The method of claim 2 wherein depositing a metal oxide surface channel on the surface overlying the well region includes depositing a metal oxide material selected from the group including indium oxide ( $\text{In}_2\text{O}_3$ ), ZnO, RuO, ITO,  $\text{La}_{x-1}\text{Sr}_x\text{CoO}_3$ .

4. The method of claim 1 further comprising:  
depositing a placeholder material overlying the surface channel;  
conformally depositing oxide;  
25 etching the placeholder material to form a gate region overlying the surface channel; and,

wherein forming a gate electrode overlying the high-k dielectric includes forming the gate electrode in the gate region.

5                   5.       The method of claim 4 further comprising:  
following the deposition of the placeholder material, lightly doped drain (LDD) processing the source and drain regions;  
wherein forming a high-k dielectric insulator overlying the surface channel includes depositing the high-k dielectric prior to the deposition of the placeholder material;  
10                   the method further comprising:  
forming sidewall insulators adjacent the surface channel, high-k dielectric insulator, and gate region; and,  
heavy ion implanting and activating the source and drain regions.

15                   6.       The method of claim 4 further comprising:  
prior to the deposition of the surface channel, lightly doped drain (LDD) processing the source and drain regions;  
heavy ion implanting and activating the source and drain  
20 regions; and,  
wherein forming a high-k dielectric insulator overlying the surface channel includes depositing the high-k dielectric following the etching of the placeholder material to form the gate region.

25                   7.       The method of claim 2 wherein depositing a metal oxide surface channel on the surface channel overlying the well region

includes depositing metal oxide to a thickness in the range in the range of 10 to 20 nanometers (nm).

8. The method of claim 2 wherein depositing a metal  
oxide surface channel on the surface channel overlying the well region  
includes depositing a metal oxide having a resistivity in the range  
between 0.1 and 1000 ohm-cm.

9. The method of claim 1 wherein forming a high-k  
dielectric insulator overlying the surface channel includes depositing a  
high-k dielectric material selected from the group including  $\text{HfO}_2$ ,  $\text{HfAlO}_x$ ,  
 $\text{ZrO}_2$ , and  $\text{Al}_3\text{O}_4$ .

10. The method of claim 1 wherein forming a high-k  
dielectric insulator overlying the surface channel includes depositing the  
high-k dielectric to a thickness in the range of 1 to 5 nm.

11. The method of claim 4 wherein depositing a  
placeholder material overlying the surface channel includes forming  
placeholder material to a first thickness with a placeholder material  
surface; and,

wherein conformally depositing oxide includes depositing  
oxide to a second thickness in the range of 1.2 to 1.5 times the first  
thickness; and,

the method further comprising:

chemical mechanical polishing (CMP) the oxide to the level of the placeholder material surface.

12. The method of claim 5 wherein forming sidewall insulators adjacent the surface channel, high-k dielectric insulator, and gate region includes forming sidewalls from a material selected from the group including  $\text{Si}_3\text{N}_4$  and  $\text{Al}_2\text{O}_3$ .

13. An ultra-shallow surface channel MOS transistor, the transistor comprising:

a source region;  
a drain region;  
a well region intervening between the source and drain with a surface;  
a surface channel overlying the well region;  
a high-k dielectric insulator overlying the surface channel;  
and,  
a gate electrode overlying the high-k dielectric layer.

14. The transistor of claim 13 wherein the surface channel is a metal oxide material.

15. The transistor of claim 14 wherein the metal oxide surface channel is a material selected from the group including indium oxide ( $\text{In}_2\text{O}_3$ ),  $\text{ZnO}$ ,  $\text{RuO}$ ,  $\text{ITO}$ ,  $\text{La}_{x-1}\text{Sr}_x\text{CoO}_3$ .

16. The transistor of claim 13 further comprising:  
a placeholder overlying the surface channel, forming a  
temporary gate region; and,  
wherein the gate electrode is formed in the gate region.

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17. The transistor of claim 16 wherein the placeholder is  
temporarily formed directly overlying the high-k dielectric insulator;  
the transistor further comprising:  
sidewall insulators adjacent the surface channel, high-k  
10 dielectric insulator, and the gate region.

18. The transistor of claim 16 wherein the placeholder is  
temporarily formed directly overlying the surface channel.

15 19. The transistor of claim 14 wherein the metal oxide  
surface channel has a thickness in the range in the range of 10 to 20  
nanometers (nm).

20 20. The transistor of claim 14 wherein the metal oxide  
surface channel has a resistivity in the range between 0.1 and 1000 ohm-  
cm.

21. The transistor of claim 13 wherein the high-k  
dielectric insulator is a material selected from the group including HfO<sub>2</sub>,  
25 HfAlO<sub>x</sub>, ZrO<sub>2</sub>, and Al<sub>3</sub>O<sub>4</sub>.

22. The transistor of claim 13 wherein the high-k dielectric insulator has a thickness in the range of 1 to 5 nm.

23. The transistor of claim 17 wherein the sidewall  
5 insulators are a material selected from the group including  $\text{Si}_3\text{N}_4$  and  $\text{Al}_2\text{O}_3$ .